The demand growth for GFLOPS has always out-paced improvements in energy efficiency; the trend is getting progressively worse!

The future of embedded computing is "hybrid" computing where each device type is used for the task that it performs most efficiently.

A Sensible Shared Memory Model

- No HW Cache:
  - Very energy inefficient
  - Hard to design cache hit rate, simply.
  - Non-determinism
  - Costs in the way

- No virtual memory:
  - Allow all programs access to whole space
  - Unrestricted sharing of data
  - 5 GB/sec Off-chip Bandwidth
  - 512 GB/sec On-chip Bandwidth
  - Speed, speed, speed: have paradigm in true binary computing
  - Pass data between cores without stalling
  - 1000x more energy efficient than interchip communication

No need to learn new architecture, just call API function from host

A Technology Comparison

As process technology scales beyond 28nm, standby leakage will become a show stopper and the most area efficient architecture will be the one surviving.

Usage Model

- ANSI-C Programmable
  - Run your existing floating point programs out of the box!
  - No special program constructs needed!
  - Native single cycle throughput floating point instruction support!

- General Purpose Programmable
  - Parallelization at math kernel level, not at instruction level
  - No SIMD or VLX vectors
  - Shared memory architecture
  - Accelerator Model
  - Can be used as a BLAS/DSP binary accelerator
  - No need to learn new architecture, just call API function from host

Architecture Prototype & Silicon Results

Availability:
- Silicon in lab confirms wafer advantage
- Currently sampling chips to lead customers

Contact information

Email: info@adapteva.com
Address: Adapteva Inc.,
1666 Massachusetts Ave, Suite 14
Lexington MA 02420
Phone: +1 (781) 325-6688
Web: http://www.adapteva.com